Listing of Claims

The following listing of claims will replace all prior versions, and listings, of claims in the subject application:

1. (currently amended) A semiconductor device, comprising:

a semiconductor substrate;

a nonvolatile memory cell that includes

a memory transistor realized by a MOS transistor including a memory gate oxide film that is arranged on the semiconductor substrate, and a floating gate made of polysilicon that is arranged on the memory gate oxide film which floating gate is in an electrically floating state; and

a selection transistor realized by a MOS transistor that is serially connected to the memory transistor, the selection transistor including a selection gate oxide film that is arranged on the semiconductor substrate, and a selection gate made of polysilicon that is arranged on the selection gate oxide film, wherein an n-type impurity is introduced into the selection gate; and

a peripheral circuit transistor realized by a MOS transistor including a peripheral circuit gate oxide film that is arranged on the semiconductor substrate, and a peripheral circuit gate made of polysilicon that is arranged on the peripheral circuit gate oxide film; wherein the memory gate oxide film is arranged to be thinner than the peripheral circuit gate oxide film,

wherein an impurity concentration of the selection gate and the peripheral circuit gate is higher than an impurity concentration of the floating gate.

2. (original) The semiconductor device as claimed in claim 1, wherein the memory transistor

and the selection transistor are PMOS transistors.

3. (original) The semiconductor device as claimed in claim 1, wherein the selection gate oxide film and the memory gate oxide film are arranged to have a same thickness.

4. (original) The semiconductor device as claimed in claim 1, wherein the selection gate oxide film and the peripheral circuit gate oxide film are arranged to have a same thickness.

5. (original) The semiconductor device as claimed in claim 1, further comprising: a capacitor including a lower electrode made of polysilicon that is arranged on the semiconductor substrate via an insulating film, and an upper electrode made of polysilicon that is arranged on the lower electrode via a capacitor insulating film;

wherein the floating gate and the lower electrode are created from a same polysilicon layer, and the capacitor insulating film is arranged on an upper surface and a side surface of the floating gate.

6. (original) The semiconductor device as claimed in claim 5, wherein the peripheral circuit gate and the upper electrode are created from a same polysilicon layer.

7. (original) The semiconductor device as claimed in claim 5, wherein the selection gate, the floating gate, and the lower electrode are created from the same polysilicon layer.

8. (original) The semiconductor device as claimed in claim 6, wherein the selection gate, the peripheral circuit gate, and the upper electrode are created from the same polysilicon layer.

Claims 9-22 (canceled).

23. (new) The semiconductor device as claimed in claim 1, wherein the n-type impurity is phosphorous.